Applicant	James D. Beasom	**AMENDMENT AND RESPONSE UNDER 37 C.F.R. §1.111**
Serial No.	09/992,880	
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Group Art Unit	2814	
Examiner Name	Hoai V. Pham	
Attorney Docket No.	125.014US01	
Title: INTEGRATED CIRCUIT WITH MOS CAPACITOR		

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on June 3, 2002. Please amend the above-identified application as follows.

IN THE CLAIMS

Please amend Claims 10, 13, 15, 23, 27, 28 as follows:

10. (Amended Once) A method of forming an integrated circuit, the method comprising:

forming an oxide layer on a surface of a substrate, the substrate having a plurality of isolation islands, wherein at least one isolation island is used in forming a semiconductor device;

patterning the oxide layer to expose predetermined areas of the surface of the substrate;

depositing a nitride layer overlaying the oxide layer and the exposed surface areas of the substrate, wherein the nitride layer is in contact with the oxide layer and all of the exposed surface areas created by the patterning of the oxide layer; and

implanting ions through the nitride layer, wherein the nitride layer is an implant screen for the implanted ions.

13. (Amended Once) The method of claim 10, further comprising:

performing a dry etch to form anisotropic contact openings that extend through the layer of nitride and through the layer of oxide to access selected device regions formed in the substrate by the implanted ions.

15. (Amended Once) A method of forming an integrated circuit, the method comprising: